IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-28. (Canceled)

29. (Currently Amended) A program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform operations for determining when to perform an error recovery instruction, the operations comprising:

receiving an error recovery instruction;

beginning a timeout task;

monitoring a processor interface to identify processor status for determining a time to perform the error recovery instruction for withholding access to [[the]] a local processor; and

performing the error recovery instruction when the monitoring determines a time for performing the error recovery instruction.

30. (Previously Presented) The program storage device of claim 28 further comprising forcing an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction.

31. (Previously Presented) The program storage device of claim 30 further comprising resuming normal operations after performing the error recovery instruction.

32. (Previously Presented) The program storage device of claim 28, wherein the monitoring a processor interface to identify processor status for determining a time to perform the error recovery instruction for withholding access to the local processor further comprises:

monitoring a processor interface to a host bus for an idle condition;

withholding access to the processor interface when the idle condition is detected;

after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle; and

identifying the time to perform the error recovery instruction when all data transfer paths are idle.

33. (Previously Presented) The program storage device of claim 32 further comprising resuming normal operations after performing the error recovery instruction.

34. (Previously Presented) The program storage device of claim 28 further comprising resuming normal operations after performing the error recovery instruction.

35. (Currently Amended) A program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform operations for determining when to perform an error recovery instruction, the operations comprising:

receiving an error recovery instruction;

monitoring a processor interface to identify processor status for determining a time to perform the error recovery instruction for withholding access to [[the]] a local processor; and

performing the error recovery instruction when the monitoring determines a time for performing the error recovery instruction.

36. (Previously Presented) The program storage device of claim 35 further comprising beginning a timeout task after receiving the error recovery instruction and forcing an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction.

37. (Previously Presented) The program storage device of claim 36 further comprising resuming normal operations after performing the error recovery instruction.

38. (Previously Presented) The program storage device of claim 35, wherein the monitoring a processor interface to identify processor status for determining a time to perform the error recovery instruction for withholding access to the local processor further comprises:

monitoring a processor interface to a host bus for an idle condition;

withholding access to the processor interface when the idle condition is detected;

after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle; and

identifying the time to perform the error recovery instruction when all data transfer paths are idle.

39. (Previously Presented) The program storage device of claim 38 further comprising resuming normal operations after performing the error recovery instruction.

40. (Previously Presented) The program storage device of claim 35 further comprising resuming normal operations after performing the error recovery instruction.

41. (Currently Amended) An apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

self-quiesce logic for receiving an error recovery instruction; and

a timer, coupled to the self-quiesce logic, for determining when to force execution of the error recovery instruction;

wherein the self-quiesce logic initiates the timer when the error recovery instruction is received, begins to monitor a processor interface to identify processor status for determining a time to perform the error recovery instruction for withholding access to [[the]] a local processor and performs the error recovery instruction when the monitoring determines a time for performing the error recovery instruction.

42. (Previously Presented) The apparatus of claim 41, wherein the self-quiesce logic forces an execution of the error recovery instruction when the timer expires before the self-quiesce logic determines a time to perform the error recovery instruction.

43. (Previously Presented) The apparatus of claim 42, wherein the self-quiesce logic allows resuming normal operations after the error recovery instruction is performed.

44. (Previously Presented) The apparatus of claim 41, wherein the self-quiesce logic monitors a processor interface to a host bus to identify processor status for determining a time to perform the error recovery instruction for withholding access to the local processor by monitoring the processor interface for an idle condition, withholding access to the processor interface when the idle condition is detected, after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle and identifying the time to perform the error recovery instruction when all data transfer paths are idle.

45. (Previously Presented) The apparatus of claim 44, wherein the self-quiesce logic allows resuming normal operations after the error recovery instruction is performed.

46. (Previously Presented) The apparatus of claim 41, wherein the self-quiesce logic allows resuming normal operations after the error recovery instruction is performed.

47. (Currently Amended) An apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

a processor for executing instructions; and

self-quiesce logic, coupled to the processor, the self-quiesce logic detecting an error recovery instruction, wherein the self-quiesce logic monitors a processor interface to identify processor status for determining a time to perform the error recovery instruction for withholding access to [[the]] a local processor and performs the error recovery instruction when the monitoring determines a time for performing the error recovery instruction.

48. (Previously Presented) The apparatus of claim 47 further comprising a timer for determining when to abort the monitoring of processor status and data path activity and cause an execution of the error recovery instruction.

49. (Previously Presented) The apparatus of claim 48, wherein the self-quiesce logic causes normal operations to be resumed after performing the error recovery instruction.

50. (Previously Presented) The apparatus of claim 47, wherein the self-quiesce logic monitors a processor interface to a host bus to identify processor status for determining a time to perform the error recovery instruction for withholding access to the local processor by monitoring the processor interface for an idle condition, withholding access to the processor interface when the idle condition is detected, after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle and identifying the time to perform the error recovery instruction when all data transfer paths are idle.

51. (Previously Presented) The apparatus of claim 50, wherein the self-quiesce logic causes normal operations to be resumed after performing the error recovery instruction.

52. (Previously Presented) The apparatus of claim 47, wherein the self-quiesce logic causes normal operations to be resumed after performing the error recovery instruction.

53. (Currently Amended) A method for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction;

beginning a timeout task;

monitoring a processor interface to identify processor status for determining a time to perform the error recovery instruction for withholding access to [[the]] a local processor; and

performing the error recovery instruction when the monitoring determines a time for performing the error recovery instruction.

54. (Currently Amended) A method for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction;

monitoring a processor interface to identify processor status for determining a time to perform the error recovery instruction for withholding access to [[the]] a local processor; and

performing the error recovery instruction when the monitoring determines a time for performing the error recovery instruction.

55. (Currently Amended) An apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

means for receiving an error recovery instruction; and

means for determining when to force execution of the error recovery instruction;

wherein the means for receiving the error recovery instruction initiates a timer when the error recovery instruction is received, begins to monitor a processor interface to identify processor status for determining a time to perform the error recovery instruction for withholding access to [[the]] a local processor and performs the error recovery instruction when a time for performing the error recovery instruction is determined.

56. (Currently Amended) An apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

means for executing instructions; and

means, coupled to the means for executing instructions, for detecting an error recovery instruction, monitoring a processor interface to identify processor status for determining a time to perform the error recovery instruction for withholding access to [[the]] a local processor and performing the error recovery instruction when a time for performing the error recovery instruction is determined.